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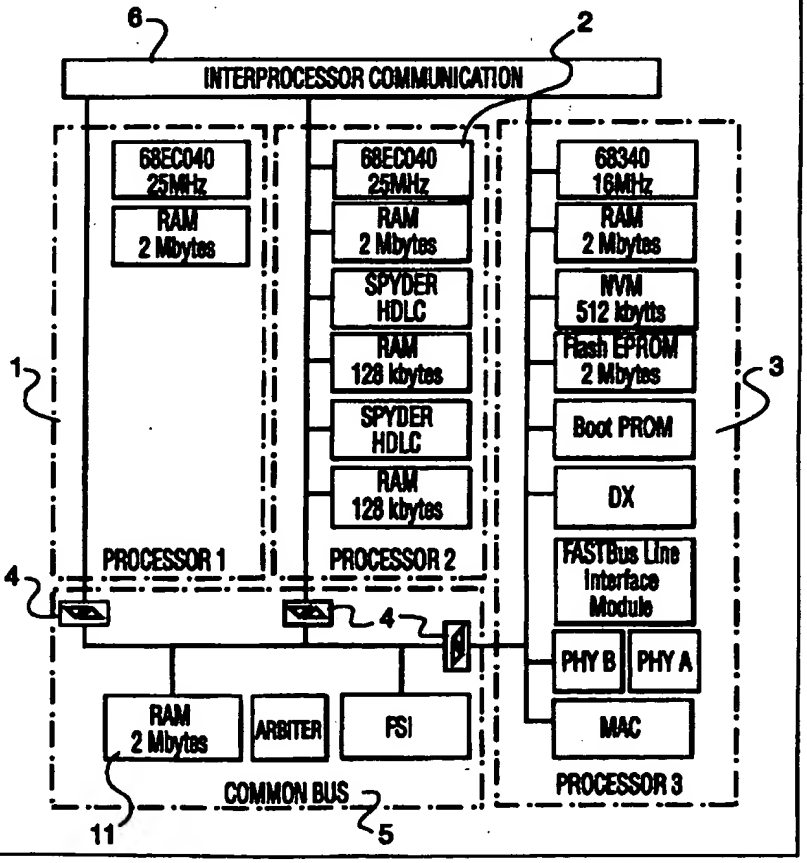
(54) Title: INTERPROCESSOR COMMUNICATIONS SYSTEM

(57) Abstract

A multiprocessor system comprises a plurality of processors attached to a common bus. A communication logic unit independent from said bus provides interprocessor cummunication. Interrupts triggered by the occurence of events signal the events via the logic unit. The source and priority of the events are identified.



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INTERPROCESSOR COMMUNICATIONS SYSTEM

This invention relates to an interprocessor communications system.

Multiprocessors require a method of communication with each other. This is essentially the ability to signal the occurrence of events between processors. Furthermore, a method of signaling several types of events must be provided.

Traditionally, this interprocessor communication has been done using flags located in memory shared by all processors in the system. A processor must then poll the flags in order to determine if there is a message or event from another processor. This leads to a bottleneck in the shared memory as well as latencies associated with the length of the polling interval, especially if several flags must be checked each time.

An object of the invention is to alleviate this problem.

According to the present invention, there is provided a multiprocessor system comprising a communications logic unit for connecting a group of processors, which provides a mechanism for signaling the occurrence of events between processors. Means are provided for generating interrupts triggered by the occurrence of events, and for identifying the source and priority of the events.

This communications logic unit may directly accessible by each processor on its local bus, thereby eliminating the shared memory bottleneck.

Once a processor has been signaled that an event has occurred, that processor will then retrieve the full event description from shared memory. Accesses to shared memory for the purposes of interprocessor communication are

therefore limited to storage and retrieval of event descriptions. Polling for events in shared memory is eliminated.

The invention will now be described in more detail, by way of example only, with reference to the accompanying drawings, in which:-

Figure 1 is a block diagram of a multiprocessor system; and

Figure 2 shows the channel connections between the different processors in the multiprocessor system.

Referring to Figure 1, the multiprocessor system accordance to the invention is arranged on a card comprising three processors 1, 2, and 3. The processors 1, 2, 3 are connected to a main bus 5 through buffers 4. The main bus 5 is connected to shared memory 11. The processors 1, 2, 3 are also connected directly to the interprocessor communication logic 6, which is implemented in a field programmable gate array (FPGA).

Referring now to Figure 2, the interprocessor communication logic 6 comprises attention control registers 7, attention status registers 8, and attention mask registers 9. The latter are output to OR gates 10, which generate the attention interrupts for the respective processors 1, 2, 3. Figure 2 shows the arrangement of channels A, B, C, D between the registers of the different processors 1, 2, 3.

The attention status register 8 of one processor, for example processor 2, is used to set the 'Attention' bit in the Attention Status Register 8 of another (target) processor, for example processor 3. There are four bits A, B, C, D between any two processors in subregisters 7a, 7b.

These are cross connected to associated subregisters 8a,8b identified with originating processor.

Each one of the bits in the subregisters is used to indicate that one of four possible events has occurred. The initiating processor records the details of the event in shared memory and then sets the appropriate attention request bit for the target processor. Reading this register yields the current state of the attention bits that is seen by the target processors. Typically, if an initiating processor reads this as a '1', it means that the target processor has yet to complete servicing of the last event; however the bit may be set again if desired. These registers are read/write. Writing a '1' to any bit will set the bit, writing a '0' to any bit has no effect. The bit fields appear differently for each processor, and are shown below:

Attention Request Registers

Processor 1	Proc 2 Attn D	Proc 2 Attn C	Proc 2 Attn B	Proc 2 Attn A	Proc 3 Attn D	Proc 3 Attn C	Proc 3 Attn B	Proc 3 Attn A
Processor 2	Proc 1 Attn D	Proc 1 Attn C	Proc 1 Attn B	Proc 1 Attn A	Proc 3 Attn D	Proc 3 Attn C	Proc 3 Attn B	Proc 3 Attn A
Processor 2	Proc 1 Attn D	Proc 1 Attn C	Proc 1 Attn B	Proc 1 Attn A	Proc 2 Attn D	Proc 2 Attn C	Proc 2 Attn B	Proc 2 Attn A

The attention status register 7 is a read/write register, and reflects the raw (i.e. unmasked) 'Attention' request bits from each other processor. When a bit is set in this register, another processor has requested its associated processor's attention for an event that has occurred. The details of the event may then be read from shared memory by the target processor. Writing a '1' to any bit in this register will clear the bit in this register as well as the corresponding bit in the initiating processor's Attention Request Register 7. This indicates that the target processor has completed processing the event. The bit fields

appear differently for each processor, and are the same as the Attention Request Register above.

The Attention Mask Register 9 provides an Attention interrupt mask, which when set to a '1', will enable interrupts from the corresponding source processor. The interrupt mask registers are read/writeable. When the Attention bit is set in the Status register, and the corresponding interrupt mask bit is set, an interrupt is generated. The mask register is cleared at Reset, disabling all interrupts. The bit fields appear differently for each processor, and are the same as the Attention Request Register above.

Claims:

1. A multiprocessor system comprising a plurality of processors attached to a common bus, characterized in that a communication logic unit independent said bus provides interprocessor communication.

2. A multiprocessor system as claimed in claim 1, characterized in that it further comprises means for signaling the occurrence of events between said processors over said communications network, means for generating interrupts triggered by the occurrence of events, and means for identifying the source and priority of events.

3. A multiprocessor system as claimed in claim 1, characterized in that said processors have direct access to said communication logic unit without the need to compete for access to shared memory.

4. A multiprocessor system as claimed in claim 2, characterized in that said communication logic unit is implemented as a field programmable gate array.

5. A multiprocessor system as claimed in claim 3, characterized in that for each processor there is provided an attention request register and an attention status register, the attention request registers communicating directly with the attention status registers of other processors.

6. A multiprocessor system as claimed in claim 5, characterized in that said status registers each contain subregisters connected to the respective attention request registers of the other processors.

7. A multiprocessor system as claimed in claim 5, characterized in that said attention request registers each contain subregisters connected to corresponding subregisters in the status request registers.

8. A multiprocessor system as claimed in claim 7, characterized in that each attention status register is connected to an attention mask register generating an attention interrupt for the associated processor.

9. A multiprocessor system as claimed in claim 1, characterized in that the communications logic unit is directly connected to each processor via its local bus.

10. A multiprocessor system as claimed in claim 8, characterized in that the attention status registers are connected to the processors through respective OR gates.

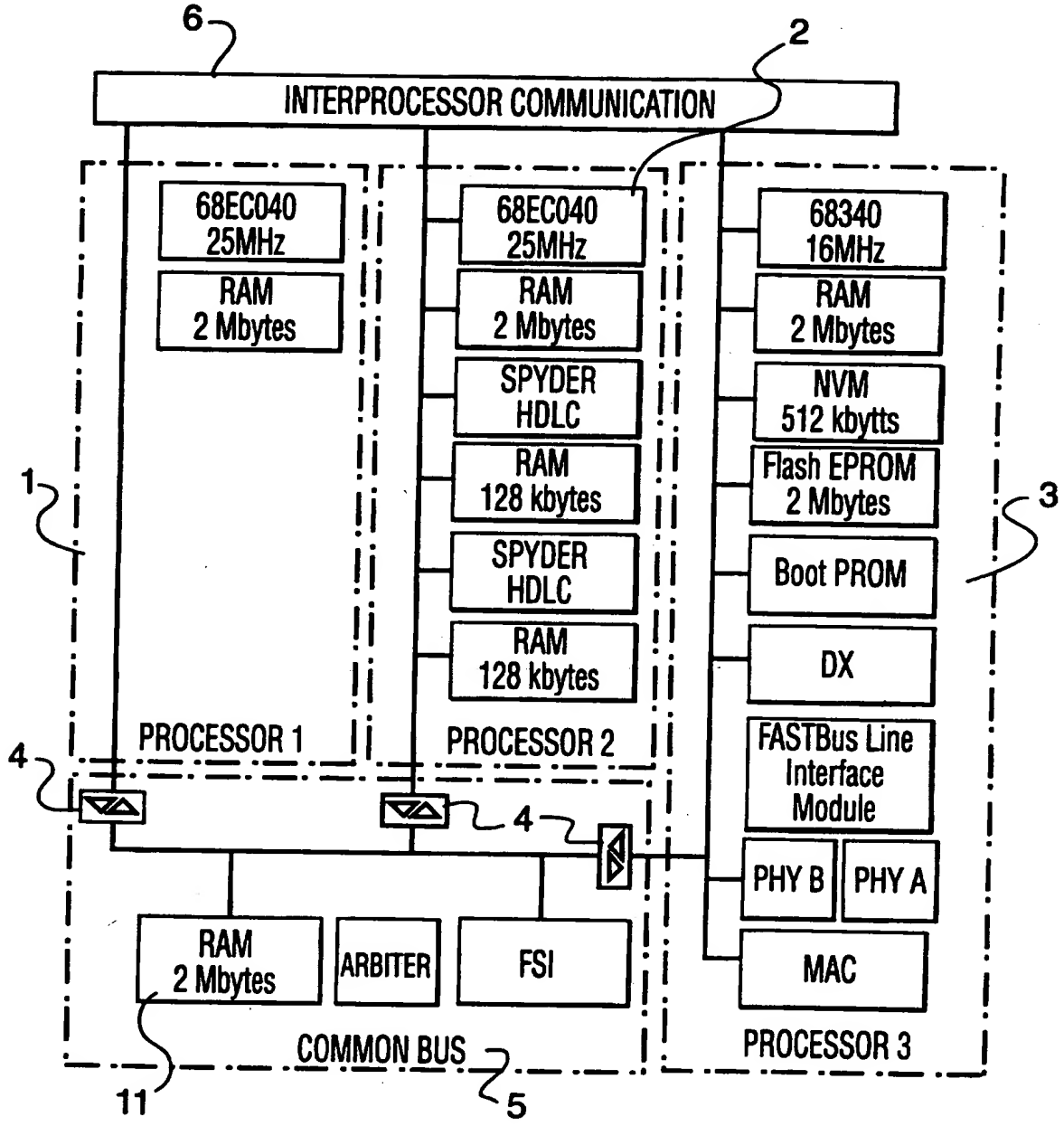
6
2
INTERPROCESSOR COMMUNICATION
68EC040 25MHz
RAM 2 Mbytes
68EC040 25MHz
RAM 2 Mbytes
SPYDER HDLC
RAM 128 kbytes
SPYDER HDLC
RAM 128 kbytes
68340 16MHz
RAM 2 Mbytes
NVM 512 kbytts
Flash EPROM 2 Mbytes
Boot PROM
DX
FASTBus Line Interface Module
PHY B
PHY A
MAC
1
3
4
4
PROCESSOR 1
PROCESSOR 2
PROCESSOR 3
RAM 2 Mbytes
ARBITER
FSI
COMMON BUS
11
5

FIG.1

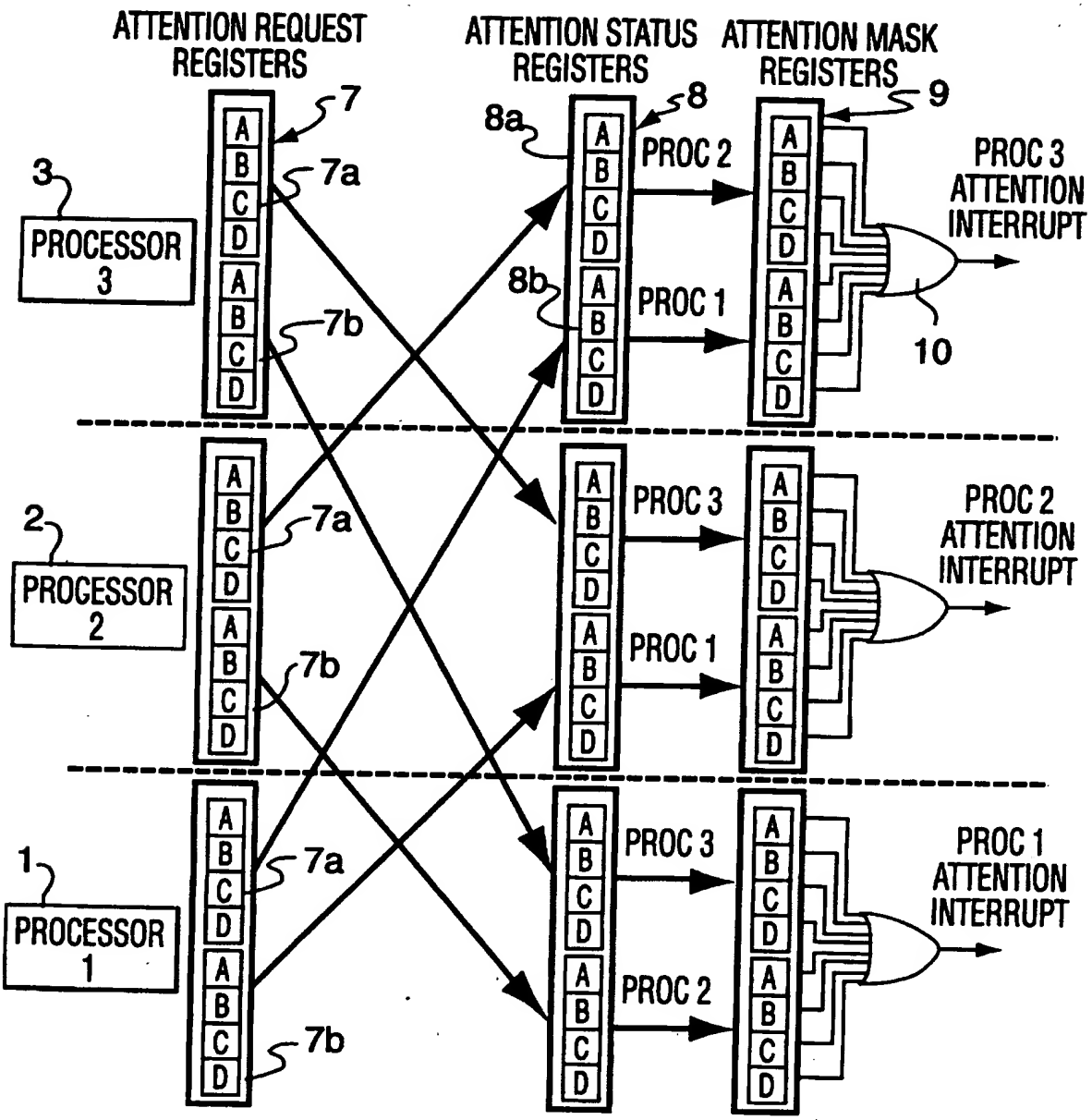
ATTENTION REQUEST REGISTERS
ATTENTION STATUS REGISTERS
ATTENTION MASK REGISTERS
7
8
9
8a
8b
10
3
PROCESSOR 3
2
PROCESSOR 2
1
PROCESSOR 1
7a
7b
PROC 2
PROC 1
PROC 3
PROC 3 ATTENTION INTERRUPT
PROC 2 ATTENTION INTERRUPT
PROC 1 ATTENTION INTERRUPT
A
B
C
D

FIG.2

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/CA 96/00172

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F15/167

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	EP,A,0 376 003 (IBM) 4 July 1990 see the whole document	1-3 4 5-10

Y	IEE PROCEEDINGS E (COMPUTERS AND DIGITAL TECHNIQUES), JULY 1983, UK, vol. 130, no. 4, ISSN 0143-7062, pages 116-124, XP002006132 DAGLESS E L ET AL: "Shared memories in the CYBA-M multimicroprocessor"	4
A	see page 119, right-hand column, line 45 - page 122, right-hand column, line 20; figures 1,6-10	1-3,5-10

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
19 June 1996	05.07.96

Name and mailing address of the ISA	Authorized officer
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	COMPUTER DESIGN, FEB. 1980, USA, vol. 19, no. 2, ISSN 0010-4566, pages 30, 32-34, XP002006133 GABLE M G: "Communications in distributed systems. I. Interfacing techniques" see page 30, right-hand column, line 17 - page 33, line 18; figure 2 ---	1
A	EP,A,0 350 911 (MODULAR COMPUTER SYST) 17 January 1990 see the whole document ---	1-10
A	EP,A,0 201 020 (HONEYWELL INF SYSTEMS) 17 December 1986 see abstract -----	1-10

1

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INTERNATIONAL SEARCH REPORT

ormation on patent family members

Interr al Application No
PCT/CA 96/00172

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		JP-B-	7095318	11-10-95
		US-A-	5210828	11-05-93
EP-A-0350911	17-01-90	NONE		
EP-A-0201020	12-11-86	CA-A-	1254663	23-05-89
		DE-A-	3687426	18-02-93
		JP-A-	61286961	17-12-86
		US-A-	4862354	29-08-89